BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

(12) UK Patent Application (19) GB (11) 2 256 293 (13) A

(43) Date of A publication 02.12.1992

(21) Application No 9111002.3

(22) Date of filing 21.05.1991

(51) INT CL[5]
G06F 12/06

(52) UK CL (Edition K)
G4A AMG1

(56) Documents cited
US 4740911 A

(58) Field of search
UK CL (Edition K) G4A AMG1 AMX
INT CL[5] G06F

(71) Applicant
Research Machines Plc

(Incorporated in the United Kingdom)

Mill Street, Oxford, OX2 0BW,
United Kingdom

(72) Inventor
Keith Alexander Ford

(74) Agent and/or Address for Service
S G Unwin & Co
2 North Street, Islip, Oxford, OX5 2SL,
United Kingdom

(54) Memory decode system

(57) A memory decode system for a computer having a plurality of memory banks each (A, B, C, D) of which is made up of a number of memory pages (1A, 2A, 1B, 2B, 1C, 2C, 1D, 2D), the system comprising a decoder module for each memory bank (A, B, C, D), each decoder module being arranged to receive memory addresses from the computer address bus and control signals and being configured to provide signals to the respective memory bank (A, B, C, D): a SELECT signal for indicating when the address supplied to the decoder module is within the address range of the respective memory bank (A, B, C, D), a HIT signal for indicating when the address supplied to the decoder module is within the address range of the memory page currently selected, and a row address signal for identifying which memory address within a given memory page is to be accessed, so as to cause the respective memory bank (A, B, C, D) to form part of a set of memory banks which are interleaved with each other on a page-by-page basis.

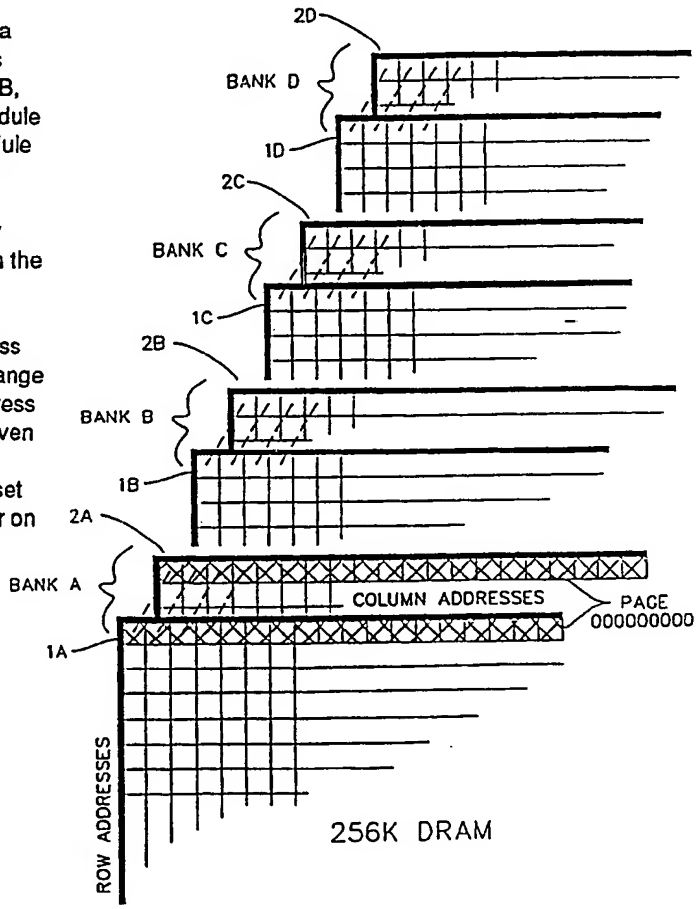

Figure 1

GB 2 256 293 A

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

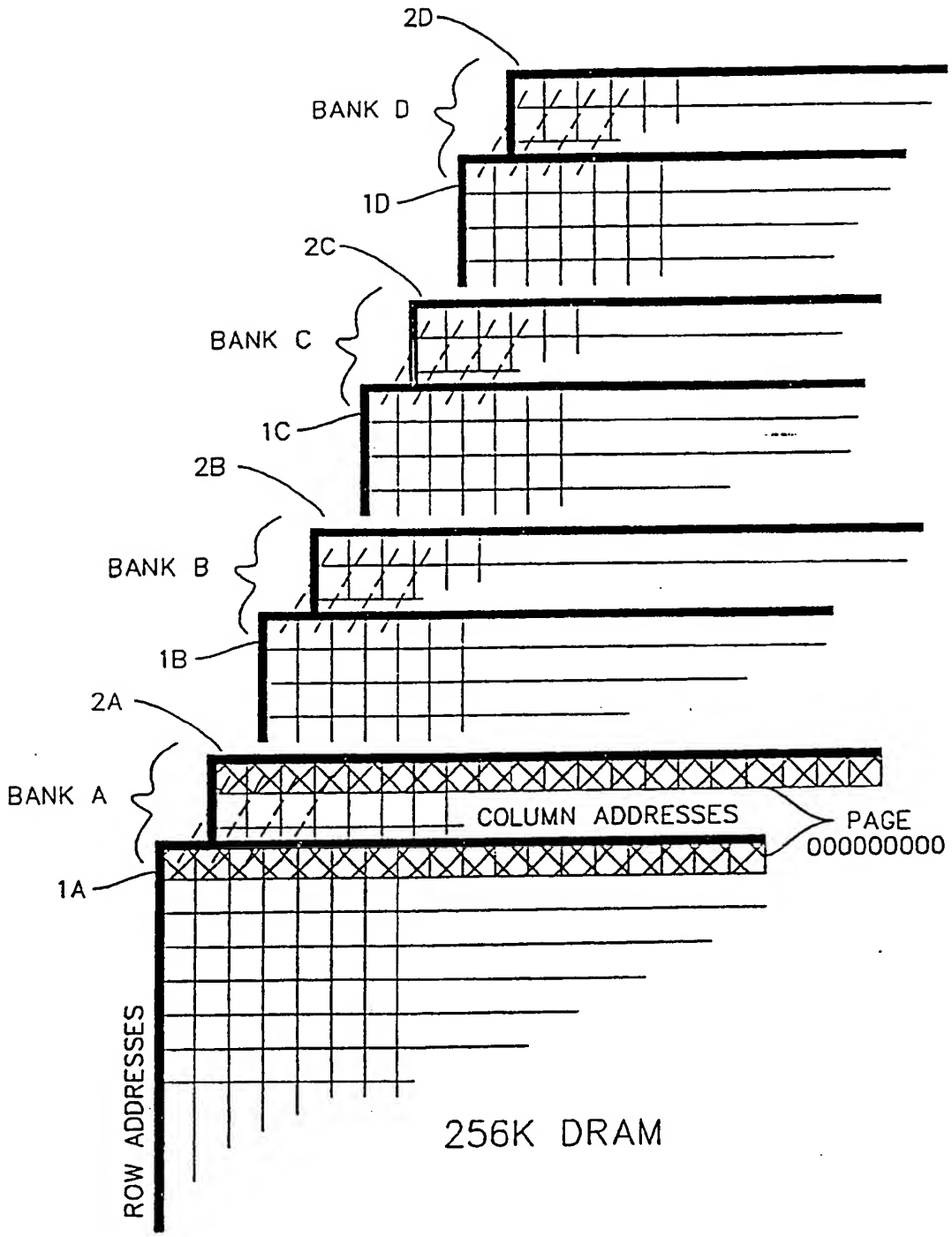

Figure 1

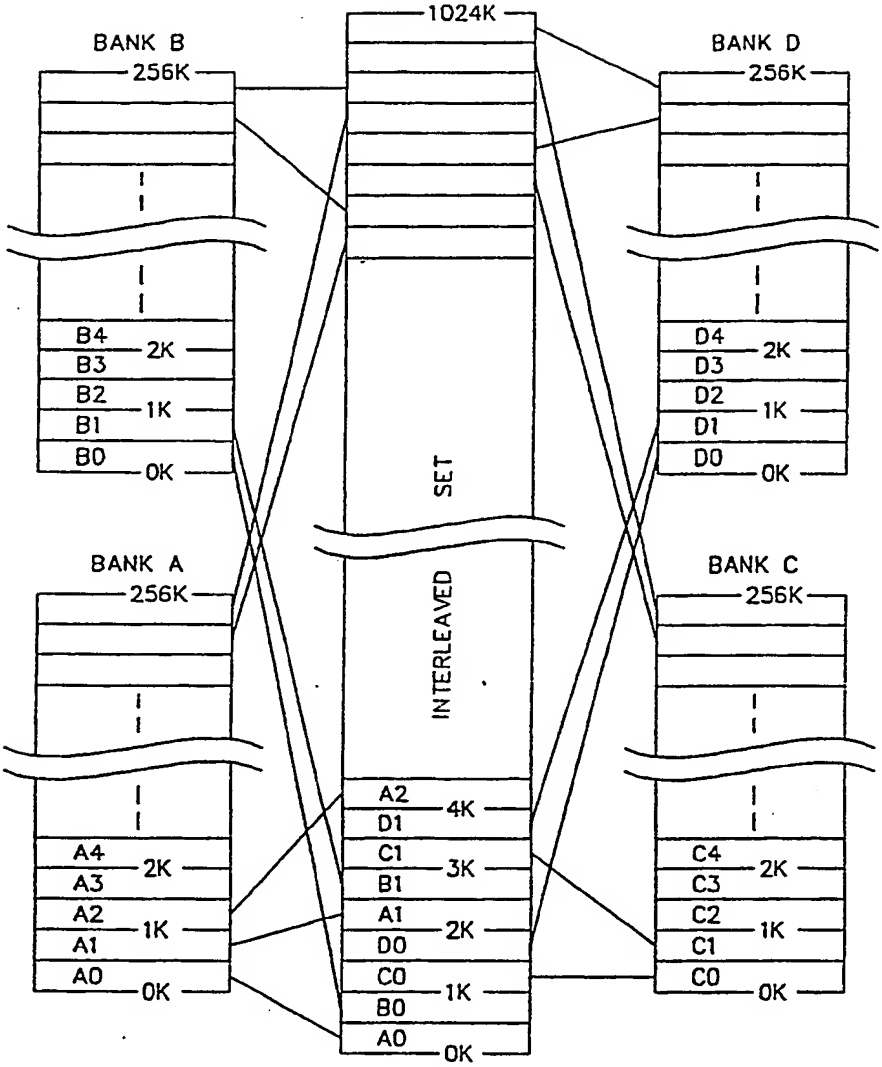

Figure 2

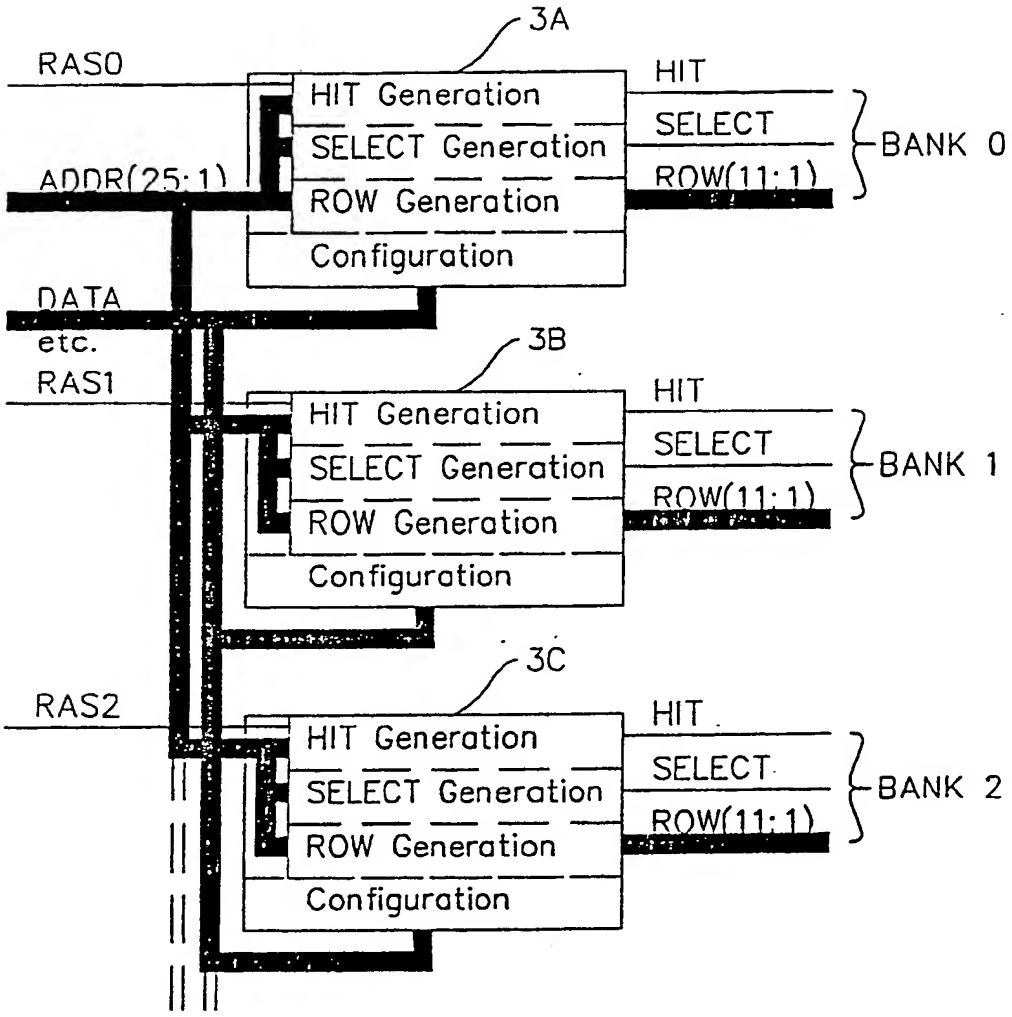

Figure 3

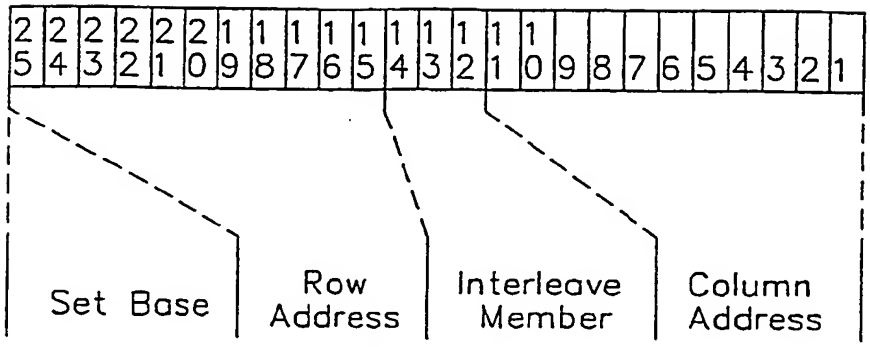

Figure 4

Address partitioning for 4M word DRAM configured for 8—way interleave

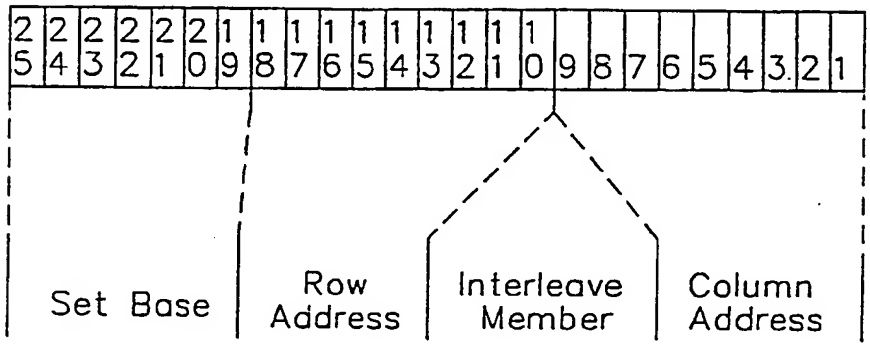

Figure 5

Address partitioning for 256K word DRAM configured for 1—way interleave

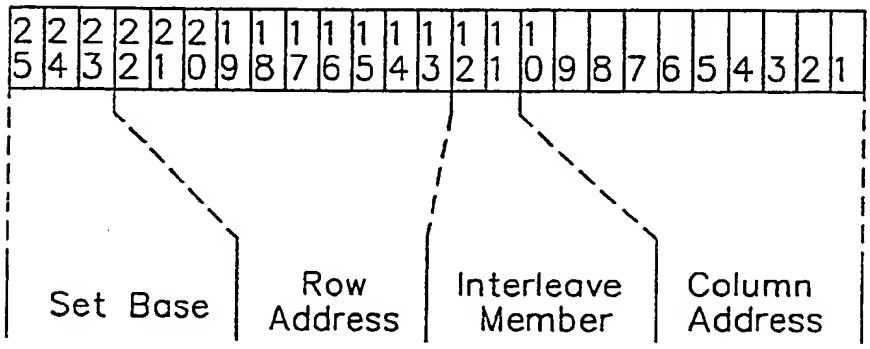

Figure 6

Address partitioning for 1M word DRAM configured for 4—way interleave

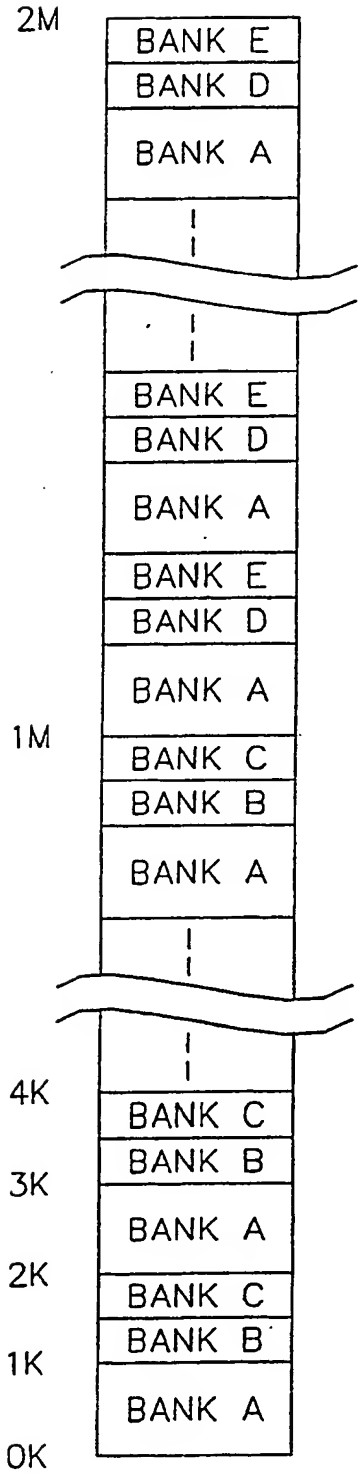

Figure 7

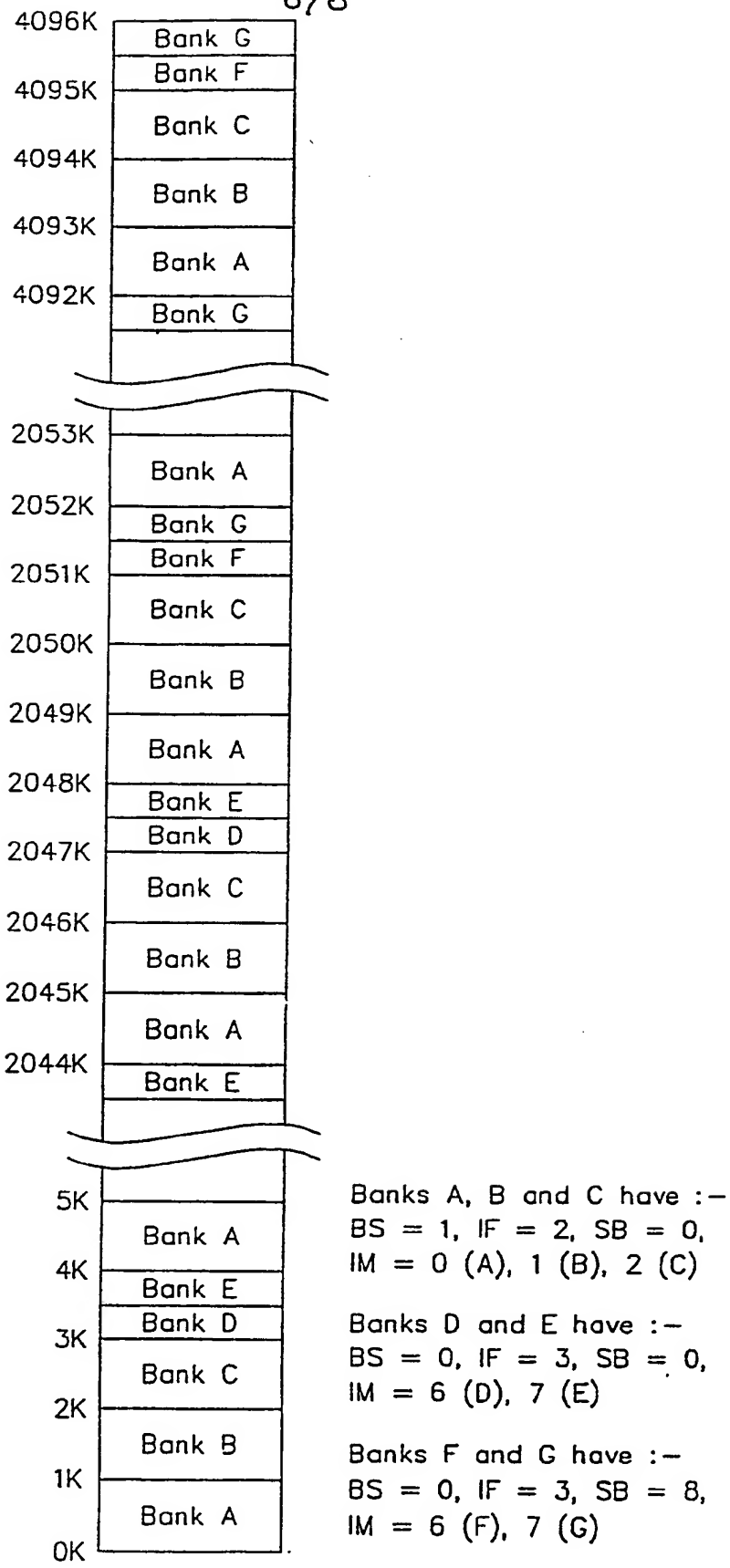

Figure 8

A 7 way, 4M word, interleave set using 3 1M word and 4 256K word DRAM banks

MEMORY DECODE SYSTEM

This invention relates to a memory decode system for a computer having a plurality of memory banks and more particularly for a digital computer incorporating a memory sub-system based on dynamic random access memory (DRAM) chips using page-mode interleaving of the DRAM for performance improvements.

Most modern microcomputers use DRAM for their main memory system and consequently require a DRAM controller. It is common for the DRAM controller to support several banks of DRAM where a bank comprises n DRAMs (where n in an integer), each comprising w words of b bits, and wired so as to behave as a single DRAM of w words of (n x b) bits. It is also common to provide the option of populating, i.e. using, only some of the total number of banks which can be supported. Thus, for example, a controller designed to support up to eight banks of DRAM may be installed in a system in which fewer than 8 banks of DRAM are actually present.

In this latter case, it is usual for the DRAM controller to provide a mechanism whereby the address decoding for the banks of DRAM can be arranged so as to provide the system with a single, contiguous block of DRAM, normally starting at address 0.

Figure 1 illustrates a memory sub-system comprising four banks (A, B, C, D) of memory in which each bank comprises two DRAMs (1A and 2A, 1B and 2B, 1C and 2C, 1D and 2D, respectively) each comprising 256K 8-bit words but wired together (as indicated by dotted lines) to behave as a single 256K 16-bit word DRAM. Each memory location in a DRAM has a row address and a column address. Thus, for a 256K, ($=2^{18}$) word DRAM there are 512 ($=2^{9}$) column addresses and 512 ($=2^{9}$) row addresses each of which comprises 9 address bits. Conventionally, the most significant bits of an address of a memory location in such a memory bank form the row address and the least significant bits form the column address. Thus, in this case, for each 18 bit address, the 9 most significant bits provide the row address and the 9 least significant bits provide the column address.

Also, as is conventional, all the addresses having the same row address are said to comprise a memory 'page'. Each page in this case thus comprises 0.5K ($=2^9$) memory locations. In the example illustrated in Figure 1, the first page of the first memory bank (A) comprises all memory locations have the row address 000000000, i.e. 0.5K 8-bit memory locations in each of the two DRAMs (1A and 2A) which are wired together to act as 0.5K 16-bit memory locations.

It is common for DRAM controllers to operate the DRAM in the, so-called, page mode whereby the most significant bits of the address which form the row address are strobed into the DRAM by a row address strobe (RAS) which is then held active. A sequence of accesses to various addresses within the selected memory page may then be made by simply strobing the column addresses with a column address strobe (CAS). Such page mode accesses are considerably faster than standard DRAM accesses and so tend, on average, to reduce the memory system access and cycle times. If an attempt is made to access a memory location which is not in the selected page then a full DRAM cycle must be run, to strobe both a new row address and a new column address.

When multiple banks of DRAM are provided, it is possible for each of their RAS lines to be driven independently so that if, for example, four banks of DRAM are present as in Figure 1 then at any one time up to four pages of DRAM (one from each bank) can be selected for page mode accesses. As most memory accesses are to an address close to that of the previous access, it is advantageous if these selected pages are close to each other in address space. This is commonly achieved by arranging the DRAM banks to be interleaved on a page-by-page basis. So, for example, in a system with four banks of DRAM of equal size arranged in a page-mode interleaved fashion, each bank provides every fourth memory page within the address space. This is illustrated in Figure 2 which shows the 0.5K memory pages of each of the four 256K word memory banks (A, B, C, D) and the manner in which the pages from the memory banks are interleaved with each other to provide an interleaved set of 1024K (=1M) words.

Such page mode interleaving has generally only been possible using a set of 2^n (where n is an integer) identical memory banks. Also, DRAM controllers supporting such page mode interleaving are normally only able to support it between specified pairs, quartets etc. of banks with a very limited number of combinations possible. A typical DRAM controller may, for instance, only allow the following configurations:

a) Bank 0 populated only with no interleave
b) Banks 0 and 1 populated with identical DRAMs with a 2-way interleave
c) Banks 2 and 3 populated with identical DRAMs with a 2-way interleave
d) Banks 0 and 1 populated with identical DRAMs with a 2-way interleave and banks 2 and 3 populated with identical DRAMs (not necessarily the same as for banks 0 and 1) with a 2-way interleave

Thus, 4-way interleaving is not provided for and the choice of banks pairs for 2-way interleaving is restricted and the only permitted non-interleaved configuration is with only bank 0 populated.

According to the invention, there is provided a memory decode system for a computer having a plurality of memory banks each of which is made up of a number of memory pages, the system comprising a decoder module for each memory bank, each decoder module being arranged to receive memory addresses from the computer address bus and control signals and being arranged to provide address and control signals to the respective memory bank in accordance with a predetermined configuration so as to cause the respective memory bank to form part of a set of memory banks which are interleaved with each other on a page-by-page basis.

Preferred features of the invention will be apparent from the following description and from the subsidiary claims of the specification.

The invention will now be further described, merely by way of example, with reference to the accompanying drawings, in which:

Figure 1 illustrates a conventional arrangement of a memory sub-system comprises a plurality of memory banks (4 in this case);

Figure 2 illustrates the manner in which memory pages of four memory banks can be interleaved on a page-by-page basis to form an interleaved set of memory banks;

Figure 3 shows a block diagram of a memory decode system according to an embodiment of the invention;

Figures 4, 5 and 6 illustrate address partitioning for three different memory sub-systems; and

Figures 7 and 8 illustrate the manner in which memory pages in two different arrangements of memory banks of different sizes can be iterleaved on a page-by-page basis to form an interleaved set of memory banks.

The memory decode system described herein provides a modular DRAM address decoder which allows a plurality of DRAM banks, including banks of different sizes, to be mapped so as to generate a single, contiguous address space whilst also allowing the maximum possible flexibility for page mode interleaving and, in some cases, the interleaving of banks of differing sizes.

The system is readily expandable to support an arbitrary number of DRAM banks with minimum added complexity and can be implementated in an application specific integrated circuit (ASIC).

The following description relates to a DRAM decoder designed to provide a memory system of up to 32M ($=2^{25}$) 16-bit words so the memory system is fed with a total of 25 address lines (numbered 1 to 25, with 1 the least significant). Up to 8 banks of DRAM (each of 256K, 1M or 4M words) are supported with up to 8-way page mode interleaving being possible. It will, however, become clear that the system could readily be modified to support any number of DRAM banks with any degree of interleaving.

As shown in Figure 3, the decode system comprises a plurality of decoder modules (3A, 3B, 3C, etc), one for each DRAM bank (not shown), all the decoder modules being identical to each other.

Each decoder module is provided with the following inputs:

an address bus (ADDR(25:1)) which provides a 25-bit signal indicating which of the 32M ($=2^{25}$) memory locations is to be accessed.

a row address strobe (RAS) signal, a control signal which causes the address bits representing a row address to be output by the module. As the largest size memory bank the system is designed to support is a 4M ($=2^{22}$) word bank (which requires 22 address bits), the row address may comprise up to 11 address bits.

data bus and control signals for configuring the module as required (as described further below).

Each decoder module is arranged to provide the following outputs:

a SELECT signal which indicates whether or not the address provided to the module is within the address range of the respective DRAM.

A HIT signal which indicates whether or not the address provided to the module is within the memory page currently selected by the RAS signal.

the row address (ROW (11:1)) of the memory location to be accessed.

Interleaved memory banks can be thought of as being combined into a number of 'interleave sets'. Each interleave set comprises 2^n (n being an integer) memory banks of the same size which are arranged to behave as a single, combined memory bank. Thus, in the example illustrated in Figure 2, the interleave set comprises 4 (2^2) memory banks (A, B, C, D) each of 256K words arranged to behave as a single 1M word memory bank.

An interleave set may be defined by the following characteristics:

Bank Size

The Bank Size indicates the size, in words, of the DRAM banks making up the interleave set, i.e. 256K, 1M or 4M in the example being considered.

Interleave Factor

The Interleave Factor indicates the repeat factor of the set, i.e. whether a page from a particular memory bank forms every second, fourth, eight etc., page in the interleaved set. Or, put more generally, it is the number of memory addresses between the addresses of successive pages from a particular bank within the interleave set divided by the number of addresses within each page. In the example shown in Figure 2, a page from each memory bank forms every fourth page of the interleave set so the Interleave Factor is 4 ($=2^2$). Or, looked at in the more general way, successive pages of a given bank are spaced at intervals of 2K addresses within the interleave set, and each page comprises 0.5K address, so the Interleave Factor is 2/0.5 = 4. It will be seen that for an interleave set of 2^n memory banks of equal size, the Interleave Factor is also 2^n.

Interleave Members

An interleave set is made up of interleaved pages from a plurality of memory banks and the order in which the pages from the different banks are interleaved is the same throughout the interleave set. An interleave set with an Interleave Factor of 2^n comprises interleaved pages from 2^n memory banks and the pages from each bank can be regarded as being numbered in dependence upon the order in which they appear in the interleave set. The Interleave Members of an interleave set of 2^n memory banks can thus be numbered 0 to $2^n - 1$. In the arrangement shown in Figure 2, the four Interleave Members are numbered 0, 1, 2 and 3 ($=2^2-1$), respectively.

Set Base Address

An interleave set of 2^n memory banks of equal size provides a contiguous block of memory of a size (S) which is 2^n times the size of each individual memory bank within the interleave set and the block of memory start at a Base Address. The Set Base Address need not

necessarily be 0 but is generally a multiple of the set size (S) and hence a multiple of the Bank Size (BS).

Each decoder module is programmed with four parameters representing these four characteristics in order to describe its operation. The four parameters, together with a Bank Enable bit are stored in an encoded form in a software accessible configuration register within the decoder module.

The Bank Size parameter (BS) is provided in encoded form as follows: 0 for 256K words, 1 for 1M words and 2 for 4M words.

The Interleave Factor parameter (IF) is provided in encloded form as follows: 0 for no interleave, 1 for an Interleave Factor of 2, 2 for an Interleave Factor of 4 and 3 for an Interleave Factor of 8 (i.e. for a set comprising 2^n banks of equal size, IF=n).

The Interleave Member parameter (IM) is provided as a number in the range of 0 to $(2^{IF}-1)$, i.e. for a set with an interleave factor parameter (IF) of 2, the Interleave Member parameters for the four members of the set are 0, 1, 2 and 3.

The Set Base address parameter (SB) indicates the base address of the interleave set and is expressed as a number of units of the smallest bank size. Thus, in the arrangement being considered, in which the total address space supported is 32M and the smallest DRAM bank size is 256K words, the largest value required for SB is given by (32M/256k) - 1 = 127. The SB parameter is thus given by a value of up to 7 bits ($127 = 2^7 - 1$).

It will therefore be seen that any system of 2^n DRAM banks of equal size can be configured to form an interleave set by setting their BS parameters at 0, 1, or 2 as appropriate, setting the IF parameters to the value n, setting the IM parameters of the individual banks to the values 0, 1, ... , 2^n-1 and setting all the SB parameters to the starting address desired for the interleave set.

Any arbitrary collection of DRAM banks can therefore be configured to form a contiguous block of memory starting at address 0 in the manner described above using the following algorithm:

Step (1) For each memory bank in turn, determine (and program the encoder accordingly) the Bank Size parameter, i.e. 0, 1, 2 or 3.

Step (2) For each Bank Size represented, count the number of banks of that size and form them into the minimum possible number of interleave sets (each set comprising 2^n members, i.e. 1, 2, 4 or 8 members etc).

Step (3) For each interleave set, calculate the size of the set, i.e. the Bank Size times the Interleave Factor.

Step (4) Sort the interleave sets in order of set size.

Step (5) Map the largest set to address 0, i.e. set its Base Address as 0, map the next largest set immediately above the first set, i.e. so its Base Address equals the size of the first set, etc.

As an example, consider a system comprising four 256K DRAM banks. Using the above algorithm, the following steps are carried out:

Step 1: Each memory bank is a 256K bank so each of the encoders is programmed with the Bank Size parameter (BS) = 0.

Step 2: Four 256K memory banks can be formed into a single interleave set of four members.

Step 3: The size of the interleave set is Bank Size (=256k) times the Interleave Factor (4 way interleave), so the size (S) of the set is 256K x 4 = IM.

Step 4: There is only one interleave set so it is the largest set.

Step 5: The interleave set is mapped with a Base Address of 0.

The above description explains how the configuration of each encoder module is programmed. The following description will explain how, once configured, the decoder module provides the output signals (HIT, SELECT and the ROW address) in response to the input signals (RAS and the 25 bit address).

To generate the SELECT, HIT and ROW signals, the 25 bit address signal must first be divided into four fields.

The column address field within the address signal is not used by the decoder module since the smallest unit of address space of interest to the decoder is a single DRAM page. As explained above, the column address field starts at the least signficant address bit (ADDR1) and its size is dependent on the size of the memory banks (and thus on the Bank Size parameter). If the Bank Size is 2^n words, each page of the bank comprises 2^n words so there are n column address bits. In the arrangement being considered, the Bank Size varies from 256K ($=2^{18}$) words to 4M ($=2^{22}$) words so that the column address field will vary from 9 bits to 11 bits in width.

The next address field is the interleave member field and is used to determine which member of an interleave set should be enabled at the current address. This field begins at the end of the column address field and so, in the arrangement being considered, starts the 10th, 11th or 12th address bit depending on the size of the column address field. The size of the interleave member field depends on the value of the Interleave Factor which in the arrangement under consideration varies from 0 to 8 ($=2^3$) and so requires between 0 and 3 bits.

The third address field is the row address field and starts immediately after the interleave member field. In the arrangement being considered, it starts anywhere between address bits 10 to 15, depending on the size of the column address field (9 to 11 bits) and the interleave member field (0 to 3 bits). The size of the row address field is the same as that of the column address field, i.e. 9 to 11 bits, and so the top address bit of this field is in the range 18 to 25.

The final field, the Set Base Address field, comprises the remaining, high order address bits and this requires from 0 to 7 bits as discussed above.

Two examples of this partitioning of the address field are illustrated in Figures 4 and 5. Figure 4 shows the situation for eight banks of 4M word DRAMs configured for 8 way interleave and Figure 5 shows the situation for a single non-interleaved 256K word bank. These two examples represent the two extreme cases. Figure 6 shows the situation for another example in this case four banks of 2M words DRAM configured for a 4-way interleave.

Having divided the 25 bit address field in this way, the manner in which the output signals of the encoder module are generated will now be described.

Generation of the row address signal (ROW)

In the simplest case of the arrangement being considered, the row address (ROW(11:1)) for the respective memory bank may be generated by means of a simple, 11 bit wide multiplexer selecting one of 6 possible sets of row address bits from the ADDR bus (the row address can start at bit 10, 11, 12, 13, 14 or 15, i.e. 6 possibilities). The address bit ADDR(a) which provides the row address bit ROW(r) is determined by the following formula:

$$a = r + 9 + IF + BS$$

where a is the number of the address bit, r is the number of the row address bit and IF and BS are the Interleave Factor and Bank Size parameters discussed above.

Thus, for the example illustrated in Figure 5 in which IF and BS are 3 and 2, respectively, $a = r + 9 + 3 + 2 = r + 14$ so row address bits 1 to 11 are provided by address bits 15 to 25.

Some logic reduction can be achieved by noting that the order in which row address bits ROW(1) to ROW(9) are connected to the DRAM address lines is unimportant as these are provided for all of the memory sizes supported. However, row address bits ROW(10) and ROW(11) are important since these are

only connected for the larger DRAM sizes (1M and 4M). As will be appreciated from Figures 4, 5 and 6, in the arrangement under consideration, address bits ADDR(15) to ADDR(18) are always connected to address lines within the range ROW(1) to ROW(9). By re-arranging the order of the ROW(n) signals to the DRAM, these ADDR(n) lines can always be connected to ROW(1) to ROW(4), thus avoiding the need for multiplexers to generate these row address bits and so reducing the width of the multiplexer required from 11 bits to 7 bits.

Similar techniques can be used to reduce the number of ways of the multiplexer for the other ROW(n) lines. The multiplexer needs to be able to switch the row address between 6 states corresponding to row addresses starting at address bits 10, 11, 12, 13, 14 and 15 as discussed above. As all these result in address bits 15 to 18 being connected to row address bits in the range 1 to 9, address bits 15 to 18 can be permanently connected to provide three of the row address bits 1 to 9. In the first three cases, address bits 13 and 14 will always form part of the row address and in the other three cases, address bits 16 and 17 will always form part of the row address. So, row bits 5 and 6 can be provided by address bits 13 and 14 in the first three cases and by address bits 16 and 17 in the other three cases.

There are, of course, many different (and equally good) combinations for assigning address bits as row address bits.

Generation of the SELECT signal

The SELECT signal indicates whether the address supplied to the decoder module is within the address range of the respective memory bank. The address range for a memory bank forming part of an interleave set comprises a series of bands of address ranges corresponding to the pages the bank provides for the interleave set. In the example illustrated in Figure 2, for instance, the address range of the memory bank A comprises the series of address bands 0K to 0.5K, 2K to 2.5K, 4K to 4.5K etc. It will therefore be seen that an address falls within such an address range if the Set Base Address field of the address matches the Set Base Address field of

the configuration register and the Interleave Member field of the address matches the Interleave Member value specified in the configuration register.

Comparison of these fields with the data stored in the configuration register may be performed using a special equality comparator in which each pair of data bits also has a 'mask' bit associated with it so a match is considered to occur if either the two data bits match each other or if the mask bit is active.

Comparison of the Set Base Address is thus made by comparing the top 7 bits of the input address with the Set Base field of the configuration register using a 7-bit wide comparator of the type described above. The 7-bit mask input is used to mask out the n least signficant bits from the comparison, where n is given by the formula:

$n = IF + (2 \times BS)$

Thus, for a non-interleaved 256K word bank (IF=0, BS=0), n is 0 and all the address bits (19 to 25 as in Figure 4) are taken into account in the comparison. At the other extreme, for a 4M word bank part of an 8-way interleave (IF=3, BS=2), n=7 and all the address bits are ignored (i.e. all 7 mask bits are active) since no address bits are used to provide the Set Base Address parameter (see Figure 5).

The Interleave Member comparison is performed using a similar 5 bit wide comparator. The address inputs to the comparator are fed with address bits ADDR(10) to ADDR(14) which are guaranteed to include the interleave member field (see Figures 4, 5 and 6). The configuration register input is generated from the Interleave Member field shifted left by BS places (i.e. 0, 1 or 2 places) and the mask input is used to mask the BS least signficant bits and the (5 - BS - IF) most significant bits of the comparison. Thus, for the Figure 4 example, the configuration register input is generated from the address bits 10 to 14 shifted left by BS (=0) places, and so from the address bits 10 to 14, and the mask input masks the BS (=0) least significant bits and the (5 - BS - IF) = 5 - 0 - 0 = 5 most signficant bits so all 5 address bits 10 to 14 are masked (since in this

example no address bits are required for the interleave member field). Similarly, for the example shown in Figure 5, the configuration register input is generated from the address bits 10 to 14 shifted left by BS (=2) place, and so from the address bits 12 to 14, and the mask input masks the BS (=2) least significant bits (bits 10 and 11) and the 5 - BS - IF = 5 - 2 - 3 = 0 most signficant bits, so all three address bits 12 to 14 are used in the comparison (corresponding to the interleave member field shown in Figure 5).

Generation of the HIT signal

The HIT signal indicates whether the address supplied to the decoder module is within the address range of the memory page currently being addressed. This occurs if the RAS line for the decoder is active and the bits of the address under test representing the row address thereof match the values the corresponding bits had at the time the RAS signal was asserted.

To achieve this a latch is required to store the value of the high order address bits at the time when the RAS signal was asserted. This is implemented by means of a 16-bit latch whose data inputs are connected to the ADDR(10) to ADDR(25) signals (the lower order address signals 0 to 9 are guaranteed to be column address bits and can therefore be ignored) and which is open (transparent) while RAS is inactive and closed when RAS is active. The output of this latch is compared with the corresponding input address bits, with address bit ADDR(10) being ignored for a 1M and address bits ADDR(10) and ADDR(11) being ignored for a 4M word bank. If there is a match and the RAS line is asserted, then the HIT signal is driven active.

The description so far has related only to the interleaving of a number (2^n) of banks of equal size. However, there are some cases in which, using this modular approach, combinations of banks of different sizes can be interleaved.

The simplest such case is a system comprising four banks (B, C, D, E) of 256K words each and one bank (A) of 1M words giving a total of 2M words of memory. If the 1M word bank (A) is set as interleave member 0 of a 2-way interleave set with base address 0, and two (B and C) of the 256K banks are

set to be members 2 and 3 of a 4-way interleave set based at 0, while the remaining two 256K banks (A and E) are set to be members 2 and 3 of a 4 way interleave set based at address 1M, the overall effect is to produce a single 2M word interleave set based at address 0 as illustrated in Figure 7.

A similar technique can be used to interleave 3 banks (A, B, C) of 1M words with 4 banks (D, E, F, G) of 256K words to form a single 4M interleave set. In this case the three 1M banks (A, B, C) are arranged as members 0, 1 and 2 of a 4-way interleave set with a base address at 0, two of the 256K banks (D and E) are set as members 6 and 7 of an 8-way interleave set with a base address at 0, and the other two 256K banks (F and G) are set as members 6 and 7 of an eight way interleave set with above address at 2M (=2048K). This case is illustrated in Figure 8.

A similar technique can be used if the 256K banks are replaced by 1M banks, the 1M banks replaced by 4M banks and all the addresses multiplied by 4.

One disadvantage of the modular approach described above in which each of the memory banks has its own, totally independent, decoder module is that it is possible to program two or more DRAM banks to share the same area of address space. This is clearly highly undesirable as it could cause bus clashes between the selected banks of DRAM. This problem, however, is readily overcome by installing, in the logic (not described herein) which generates the DRAM control signals, a circuit which detects the simultaneous activation of two or more bank SELECT or HIT signals and, if this occurs, inhibits the generation of the column address strobe (CAS) to all banks of DRAM.

A DRAM controller can be implemented in two significantly different ways using the address decode system described above using ASIC technology.

In a first arrangement, a single chip may be built which incorporates a number of decoder modules (e.g. 8) together with the control logic necessary to generate DRAM address and control signals. A multiplexer is also provided to select the ROW address from whichever decoder module is

generating an active SELECT signal to provide the DRAM row address. This approach results in a DRAM controller chip which, although it has very flexible control over DRAM interleaving, still only supports a fixed, maximum number of banks of DRAM in the same way as conventional memory decode systems.

A second arrangement is to integrate a single bank decoder module, together with an address multiplexer to generate a multiplexed row/column address, and the control logic necessary to generate the control signals for a single DRAM bank, on a chip. The chip is thus a self-contained DRAM controller for a single bank of DRAM - although it can still be used to cause the DRAM bank to appear as a member of an interleaved set of banks. With such an arrangement there is no reason (except for the fan-out of the signals being input to the DRAM controllers) why the total memory system should not be extended to an arbitrarily large number of DRAM banks (although the maximum interleave factor is still pre-determined by the design of the decoder module).

The memory decode system described above provides a flexible, modular means for arranging multiple banks of DRAMs of varying sizes to be interleaved on a page-by-page basis to provide a contiguous address space to assist in maximising the performance of the memory sub-system.

CLAIMS

1. A memory decode system for a computer having a plurality of memory banks each of which is made up of a number of memory pages, the system comprising a decoder module for each memory bank, each decoder module being arranged to receive memory addresses from the computer address bus and control signals and being arranged to provide address and control signals to the respective memory bank in accordance with a predetermined configuration so as to cause the respective memory bank to form part of a set of memory banks which are interleaved with each other on a page-by-page basis.

2. A system as claimed in claim 1 in which each decoder module is arranged to provide the following signals to the respective memory bank: a SELECT signal for indicating when the address supplied to the decoder module is within the address range of the respective memory bank, a HIT signal for indicating when the address supplied to the decoder module is within the address range of the memory page currently selected and a row address signal for identifying which memory address within a given memory page is to be accessed.

3. A system as claimed in claim 2 in which each decoder module is arranged to define the respective memory bank's part in the interleaved set by means of the following parameters:

a Bank Size parameter (BS) representing the size, in words, of the respective memory bank;

an Interleave Factor parameter (IF) representing the repeat factor of the interleave set defined by the number of memory addresses between the addresses of successive pages from the respective memory bank within the set divided by the number of addresses making up a page of the memory bank;

an Interleave Member parameter (IM) representing the order in which pages of the respective memory banks are interleaved within the set; and

a Set Base Address parameter (BA) representing the base address of the interleave set.

4. A system as claimed in claim 3 in which each module is arranged to define the respective memory bank's part in an interleaved set of 2^n memory banks (n being an integer) with the respective parameters being defined as follows:

the Bank Size parameter (BS) is set as 0, 1, 2 ... etc. depending on the size w of the respective memory bank in words, e.g. if w is 256K, 1M, 4M ... etc.

the Interleave Factor parameter (IF) is set as n.

the Interleave Member parameter (IM) is set as 0, 1, 2, 3 ... etc. depending whether pages of the respective memory bank forms every first, second, third, fourth ... etc. page of the interleaved set.

the Set Base Address parameter (BA) is set as N when the base address of the interleave set is Nw (where N is an integer).

5. A system as claimed in claim 4 which is designed to support a memory sub-system of up to 2^M words (where M is an integer) and so requires a memory address of M bits and in which each decoder module is arranged to partition the memory address into the following fields:

a column address field comprising b bits, where b is an integer and the respective memory bank comprises 2^{2b} words;

an interleave member field whose size, in bits, is equal to the value of the Interleave Factor parameter (IF);

a row address field comprising b bits; and

a set base address field comprising up to s bits where s is the number of bits required to give the value $(2^M/w_1) - 1$ in binary, where w_1 is the size of the smallest memory bank supported by the system,

wherein $(2b + IF + s) \leq M$.

6. A system as claimed in claim 5 in which each decoder module comprises a multiplexer connected to receive the address signal and arranged to generate the row address signal in dependence upon the values of b, IF and BS.

7. A system as claimed in claim 5 or 6 in which each decoder module comprises comparators arranged to generate the SELECT signal when a match between the interleave member field of the address and the value represented by the Interleave Factor parameter (IF) and a match between the set base address field of the address and the Set Base Address parameter (BA) is detected.

8. A system as claimed in claim 5, 6 or 7 in which each decoder module comprises a comparator arranged to generate the HIT signal when a match between all bits of the address under test, apart from the b column address bits, with the corresponding bits of the current address is detected.

9. A system as claimed in any preceding claim implemented on a single chip which comprises a plurality of decoder modules, control logic for generating the memory address and control signals and a multiplexer for connecting the SELECT signals from the decoder modules to the memory banks.

10. A system as claimed in any of claims 1 to 8 in which a single decoder module together with an address multiplexer for generating a multiplexed row/column address and control logic for generating control signals for a single memory bank is implemented on a chip.

11. A memory decoder system for a computer substantially as hereinbefore described with reference to the accompanying drawings.

12. Any novel feature or combination of features disclosed herein.

Amendments to the claims have been filed as follows

1. A memory decode system for a computer having a plurality of memory banks each of which is made up of a number of memory pages, the system comprising a decoder module for each memory bank, each decoder module being arranged to receive memory addresses from the computer address bus and control signals and being configured to provide the following signals to the respective memory bank: a SELECT signal for indicating when the address supplied to the decoder module is within the address range of the respective memory bank, a HIT signal for indicating when the address supplied to the decoder module is within the address range of the memory page currently selected and a row address signal for identifying which memory address within a given memory page is to be accessed so as to cause the respective memory bank to form part of a set of memory banks which are interleaved with each other on a page-by-page basis.

2. A system as claimed in claim 1 in which each decoder module is arranged to define the respective memory bank's part in the interleaved set by means of the following parameters:

a Bank Size parameter (BS) representing the size, in words, of the respective memory bank;

an Interleave Factor parameter (IF) representing the repeat factor of the interleave set defined by the number of memory addresses between the addresses of successive pages from the respective memory bank within the set divided by the number of addresses making up a page of the memory bank;

an Interleave Member parameter (IM) representing the order in which pages of the respective memory banks are interleaved within the set; and

a Set Base Address parameter (BA) representing the base address of the interleave set.

3. A system as claimed in claim 2 in which each module is arranged to define the respective memory bank's part in an interleaved set of 2^n memory banks (n being an integer) with the respective parameters being defined as follows:

the Bank Size parameter (BS) is set as 0, 1, 2 ... etc. depending on the size w of the respective memory bank in words, e.g. if w is 256K, 1M, 4M ... etc.

the Interleave Factor parameter (IF) is set as n.

the Interleave Member parameter (IM) is set as 0, 1, 2, 3 ... etc. depending whether pages of the respective memory bank forms every first, second, third, fourth ... etc. page of the interleaved set.

the Set Base Address parameter (BA) is set as N when the base address of the interleave set is Nw (where N is an integer).

4. A system as claimed in claim 3 which is designed to support a memory sub-system of up to 2^M words (where M is an integer) and so requires a memory address of M bits and in which each decoder module is arranged to partition the memory address into the following fields:

a column address field comprising b bits, where b is an integer and the respective memory bank comprises 2^{2b} words;

an interleave member field whose size, in bits, is equal to the value of the Interleave Factor parameter (IF);

a row address field comprising b bits; and

a set base address field comprising up to s bits where s is the number of bits required to give the value $(2^M/w_1) - 1$ in binary, where w_1 is the size of the smallest memory bank supported by the system,

wherein $(2b + IF + s) \leq M$.

5. A system as claimed in claim 4 in which each decoder module comprises a multiplexer connected to receive the address signal and arranged to generate the row address signal in dependence upon the values of b, IF and BS.

6. A system as claimed in claim 4 or 5 in which each decoder module comprises comparators arranged to generate the SELECT signal when a match between the interleave member field of the address and the value represented by the Interleave Factor parameter (IF) and a match between the set base address field of the address and the Set Base Address parameter (BA) is detected.

7. A system as claimed in claim 4, 5 or 6 in which each decoder module comprises a comparator arranged to generate the HIT signal when a match between all bits of the address under test, apart from the b column address bits, with the corresponding bits of the current address is detected.

8. A system as claimed in any preceding claim implemented on a single chip which comprises a plurality of decoder modules, control logic for generating the memory address and control signals and a multiplexer for connecting the SELECT signals from the decoder modules to the memory banks.

9. A system as claimed in any of claims 1 to 7 in which a single decoder module together with an address multiplexer for generating a multiplexed row/column address and control logic for generating control signals for a single memory bank is implemented on a chip.

10. A memory decoder system for a computer substantially as hereinbefore described with reference to the accompanying drawings.

11. Any novel feature or combination of features disclosed herein.

12. A memory decode system for a computer having a plurality of memory banks each of which is made up of a number of memory pages, the

system comprising a decoder module for each memory bank, each decoder module being arranged to receive memory addresses from the computer address bus and control signals and being arranged to provide address and control signals to the respective memory bank in accordance with a predetermined configuration so as to cause the respective memory bank to form part of a set of memory banks which are interleaved with each other on a page-by-page basis.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

Application number
9111002.3

Relevant Technical fields

(i) UK Cl (Edition K) G4A AMG1,AMX

(ii) Int Cl (Edition 5) G06F

Search Examiner
M J JONES

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search
10 SEPTEMBER 1991

Documents considered relevant following a search in respect of claims 1-11

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
X	US 4740911 (ELXSI)	1

SF2(p)

1gp - c:\wp51\doc99\fil000106

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).

Published 1992 at The Patent Office, Concept House, Cardiff Road, Newport, Gwent NP9 1RH. Further copies may be obtained from Unit 6, Nine Mile Point, Cwmfelinfach, Cross Keys, Newport, NP1 7HZ. Printed by Multiplex techniques ltd, St Mary Cray, Kent.

BNSDOCID: <GB___2256293A__I_>